Refine Search

10/677,008

Search Results -

Terms	Documents
pcmo and pressure and (chlorine or chloride) and argon and oxygen	1

Database:
US Pre-Grant Publication Full-Text Database
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EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L17

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Search History

DATE: Tuesday, September 21, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L17	pcmo and pressure and (chlorine or chloride) and argon and oxygen	1	L17
L16	pcmo near stack	0	L16
L15	L12 and (argon or ar)	6	L15
L14	L12 and (argon or ar)	6	L14
L13	L8 and pcmo	0	L13
L12	L8 and (flow adj rate) and (pressure) and Torr	6	L12
L11	L8 and (flow adj rate) and (pressure) and Torr and (rf adj bias)	0	L11
L10	L8 and (flow adj rate) and (pressure) and Torr and (rf adj bias) and microwave	0	L10
L9	L8 and (flow adj rate) and (pressure) and Torr and (rf ajd bias) and microwave	0	L9
L8	(titanium or ti) and ((dry adj etching) near5 electrode) and (bottom adj electrode) and (hard adj mask)	12	L8

L7	(titanium or ti) and ((dry adj etching) near5 electrode) and (bottom ajd electrode) and (hard adj mask)	0	L7
L6	L5 and patterning	3	L6
L5	L2 and photoresist	4	L5
L4	L2 and (hard adj mask)	1	L4
L3	L2 and (dry adj etching)	1	L3
L2	pcmo	69	L2
L1	pcmo adj stack	0	L1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 6774054 B1

L3: Entry 1 of 1 File: USPT Aug 10, 2004

US-PAT-NO: 6774054
DOCUMENT-IDENTIFIER: US 6774054 B1

TITLE: High temperature annealing of spin coated Pr1-xCaxMnO3 thim film for RRAM application

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWIC | Draw D

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Terms	Documents
L2 and (dry adj etching)	1

Display Format: TI Change Format

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Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 6774004 B1

L4: Entry 1 of 1 File: USPT Aug 10, 2004

US-PAT-NO: 6774004
DOCUMENT-IDENTIFIER: US 6774004 B1

TITLE: Nano-scale resistance cross-point memory array

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw. D

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Terms	Documents
L2 and (hard adj mask)	1

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 6746910 B2

L6: Entry 1 of 3 File: USPT Jun 8, 2004

US-PAT-NO: 6746910
DOCUMENT-IDENTIFIER: US 6746910 B2

TITLE: Method of fabricating self-aligned cross-point memory array

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 2. Document ID: US 6723643 B1

L6: Entry 2 of 3 File: USPT Apr 20, 2004

US-PAT-NO: 6723643
DOCUMENT-IDENTIFIER: US 6723643 B1

TITLE: Method for chemical mechanical polishing of thin films using end-point indicator structures

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 3. Document ID: US 6583003 B1

L6: Entry 3 of 3 File: USPT Jun 24, 2003

US-PAT-NO: 6583003
DOCUMENT-IDENTIFIER: US 6583003 B1

TITLE: Method of fabricating 1T1R resistive memory array

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L5 and patterning	3

Display Format: TI Change Format

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L6: Entry 1 of 3 File: USPT Jun 8, 2004

DOCUMENT-IDENTIFIER: US 6746910 B2
TITLE: Method of fabricating self-aligned cross-point memory array

Abstract Text (1):
A method of fabricating a self-aligned cross-point memory array includes preparing a substrate, including forming any supporting electronic structures; forming a p-well area on the substrate; implanting ions to form a deep N.sup.+ region; implanting ions to form a shallow P+ region on the N.sup.+ region to form a P+/N junction; depositing a barrier metal layer on the P+ region; depositing a bottom electrode layer on the barrier metal layer; depositing a sacrificial layer or silicon nitride layer on the bottom electrode layer; patterning and etching the structure to remove portions of the sacrificial layer, the bottom electrode layer, the barrier metal layer, the P+ region and the N.sup.+ region to form a trench; depositing oxide to fill the trench; patterning and etching the sacrificial layer; depositing a PCMO layer which is self-aligned with the remaining bottom electrode layer; depositing a top electrode layer, patterning and etching the top electrode layer, and completing the memory array structure.

Brief Summary Text (4):
Perovskite metal oxide thin films, such as Pr.sub.0.7 Ca.sub.0.3 MnO.sub.3 (PCMO) thin films, have reversible resistance change properties, which can be used in non-volatile memory devices for information storage. Known methods to induce the resistance change include application of a short electric pulse for writing and a long electric pulse for resetting, wherein both electric pulses have the same polarity.

Brief Summary Text (5):
PCMO thin films exhibit reversible resistance change when an electric pulse is applied. A PCMO thin film has been grown on both epitaxial YBa.sub.2 Cu.sub.3 O.sub.7 (YBCO) and partial applied. A PCMO thin film has been grown on both epitaxial YBa.sub.2 Cu.sub.3 O.sub.7 (YBCO) and partial epitaxial platinum substrates via pulsed laser ablation (PLA) technique, Liu et al., Electric-pulse-induced reversible resistance change effect in magnetoresistive films, Applied Physics Letters, 76, 2749, 2000; and Liu et al., U.S. Pat. No. 6,204,139, granted Mar. 20, 2001, for Method of switching the properties of perovskite materials used in thin film resistors. X-Ray diffraction (XRD) polar figures confirm the epitaxial properties of PCMO thin films.

Brief Summary Text (6):
U.S. Pat. No. 6,204,139 describes the resistance change which occurred when electric pulses were applied at room temperature to PCMO thin films. The PCMO thin films were deposited on both epitaxial YBa.sub.2 Cu.sub.3 O.sub.7 (YBCO) and partial epitaxial platinum substrates by pulsed laser deposition (PLD). The polarity of the electric pulse determines the character of the resistance change, i.e., increase or decrease.

Brief Summary Text (7):
An electrically programmable resistance, non-volatile memory device, operable at room temperature, was made of PCMO epitaaially grown on YBCO on LaAlO.sub.3, as published by Liu et al, however, the sample size was on the order of hundred of

microns square, which is not practical for commercial production. This type of memory may be reversibly programmed by a reversed short electrical pulse. The memory cell is able to produce either single bit or multi-bit information. However, the PCMO must be in crystalline form, which requires that the PCMO must be grown on a specific bottom electrode, such as YBCO, which is not compatible to the state-of-the-art silicon integrated circuit technology. The growth, or crystallization, temperature is relatively high, e.g., >700.degree. C., which makes integration of the device into state-of-the-art integrated circuit very complex. In addition it is not possible to cover the full circuit area with a single grain of PCMO. As the properties of a memory cell which is fabricated on a single grain PCMO crystal and the properties of a memory cell which is fabricated on a multi-grain PCMO crystal, which covers the grain boundary area, are not the same, circuit yield and memory performance problems will occur. A low .DELTA.R/R ratio was reported for the Liu et at. sample. It is not believed that the Liu et al. technique can be applied to commercially manufactured non-volatile memory devices.

Brief Summary Text (10):
A method of fabricating a self-aligned cross-point memory array includes preparing a substrate, including forming any supporting electronic structures; forming a swell area on the substrate; implanting ions to form a deep N.sup.+ region; implanting ions to form a shallow P+ region on the N.sup.+ region to form a P+/N junction; depositing a barrier metal layer on the P+ region; depositing a bottom electrode layer on the barrier metal layer; depositing a sacrificial layer of polysilicon or silicon nitride on the bottom electrode layer; patterning and etching the structure to remove portions of the polysilicon layer, the bottom electrode layer, the barrier metal layer, the P+ region and the N.sup.+ region to form a trench; depositing oxide to fill the trench; patterning and etching the polysilicon; depositing a PCMO layer which is self-aligned with the remaining bottom electrode layer; depositing a top electrode layer; patterning and etching the top electrode layer; and completing the memory array structure.

Brief Summary Text (11):
It is an object of the invention to provide a high density cross point resistor memory array having isolated PCMO cell pillars self-aligned to the bottom electrode.

Detailed Description Text (2):
This invention is a method of fabrication of a trench-isolated version of cross-point memory array, having an isolated colossal magnetoresistive oxide (CMR) cell resistor pillars, which, in the preferred embodiment, are formed on a perovskite material, such as Pr.sub.0.7 Ca.sub.0.3 MnO.sub.3 (PCMO). The structure is able to achieve high device density and may be fabricated by processes compatible with state-of-the-art ULSI techniques.

Detailed Description Text (3):
The fabrication method of the invention, and now referring to FIG. 1, includes preparation of a suitable substrate and fabrication of the non-memory devices, which will be called "supporting electronics," by any state-of-the-art process, before fabrication of the PCMO pillar. The memory array is fabricated on a substrate 10 having a p-well area 11. The entire memory area is implanted with phosphorus to form a deep N.sup.+ region 12. The energy of phosphorus ions for implantation is between about 60 keV to 200 keV and the ion dose is between about 5.multidot.10.sup.14 ions/cm.sup.-2 to 2.multidot.10.sup.15 ions/cm.sup.-2. Multi energy phosphorus may be used to reduce the resistivity of the N.sup.+ layer, and requires implantation of phosphorus ions at an energy level of between about 100 keV to 250 keV and a dose of between about 1.multidot.10.sup.14 ions/cm.sup.-2 to 2.multidot.10.sup.15 ions/cm.sup.-2. A shallow layer 14 is implanted to form a P.sup.+ /N junction. The shallow P.sup.+ layer may be implanted with BF.sub.2 ions at an energy level of between about 20 keV to 60 keV and a dose of between about 1.multidot.10.sup.15 ions/cm.sup.-2 to 5.multidot.10.sup.15 ions/cm.sup.-2.

Detailed Description Text (5):
Referring now to FIG. 2, photoresist is deposited to pattern the active area. The structure is etched to remove portions of sacrificial layer 20, portions of bottom electrode 18, portions of barrier metal 16 and portions of P.sup.+ silicon 14 and N.sup.+ silicon 12. The photoresist is then removed. The etching process etches through N.sup.+ silicon 12 into at least 10 nm of P-well 11. Any etch damage is cleaned and the etched trenches filled with oxide, which is then smoothed by CMP. FIG. 3 depicts the cross-section of FIG. 2 following the preceding steps.

Detailed Description Text (6):
Turning now to FIG. 3, photoresist is deposited to protect the memory cell area. Sacrificial layer 20, bottom electrode 18, barrier metal 16 and P.sup.+ layer 14 are etched, which may slightly etch into N.sup.+ region 12. The photoresist is removed, and a layer of oxide 22 is deposited and smoothed by CMP. A top view of the structure at this stage is depicted in FIG. 4, and a cross-section along line 5--5 is depicted in FIG. 4. A cross section along line 6--6 is depicted in FIG. 6. FIG. 7 depicts the sacrificial layer which has not yet been replaced by PCMO, and is taken along line 7--7 of FIG. 4.

Detailed Description Text (7):
Sacrificial layer 20 is again etched and PCMO memory resistance material 28 is deposited and smoothed by CMP. A top electrode layer 30 is deposited and patterned with photoresist. The top electrode is etched, and the photoresist removed, resulting in the structure of FIGS. 8-10. FIG. 8 is a top plan view of a cross-point memory array structure, wherein some metal layers and over coating are not shown. Oxide element 22 surrounds what will become PCMO resistor pillars, such as 24. In the view shown, a barrier metal layer 26 is depicted. A top electrode 28 would overly 24. FIG. 9 is a cross section view along line 9--9 of FIG. 8, depicting oxide element 22, brevet PCMO resistor pillars 24, p-well 11, N.sup.+ layer 12, P.sup.+ layer 14, barrier metal layer 16, bottom electrode 18, a PCMO layer 28 and a top electrode 30. FIG. 10 is a cross section view along line 10--10 of FIG. 8. As shown in the figures, the CMR memory pillar of each memory cell is isolated and is self-aligned to the bottom electrode, however, the top electrode and the CMR pillars are not self-aligned, thus the CMR resistance pillars are partially self-aligned with the other elements of the structure. The device is completed by fabrication of additional supporting electronics and metallization.

CLAIMS:

1. A method of fabricating a self-aligned cross-point memory array, comprising: preparing a substrate, including forming supporting electronic structures; forming a p-well area on the substrate; implanting ions to form a deep N.sup.+ region; implanting ions to form a shallow P+ region on the N.sup.+ region; depositing a barrier meal layer on the P+ region; depositing a bottom electrode layer on the barrier metal layer; depositing a sacrificial layer on the bottom electrode layer; patterning and etching to move portions of the sacrificial layer, the bottom electrode layer, the barrier metal layer, the P+ region and the N.sup.+ region to form a trench; depositing oxide to fill the trench, thereby forming plural P+/N junction; patterning and etching to remove portions of the sacrificial layer; depositing a PCMO layer which is self-aligned with the remaining bottom electrode layer; depositing a top electrode layers; patterning and etching the top electrode layer; and completing the self-aligned cross-point memory array.

2. The method of claim 1 which includes formation of additional electronic structures and metallization after said patterning and etching the top electrode layer.

10. A method of fabricating a self-aligned cross-point memory array having a partially aligned PCMO resistor pillar, comprising: preparing a substrate,

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☐ 1. Document ID: US 4304719 A

L17: Entry 1 of 1 File: USPT Dec 8, 1981

US-PAT-NO: 4304719
DOCUMENT-IDENTIFIER: US 4304719 A

TITLE: Conducting iodine-doped fluorometallophthalocyanines

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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Terms	Documents
pcmo and pressure and (chlorine or chloride) and argon and oxygen	1

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1. Document ID: US 6749770 B2

L22: Entry 1 of 6 File: USPT Jun 15, 2004

US-PAT-NO: 6749770
DOCUMENT-IDENTIFIER: US 6749770 B2

TITLE: Method of etching an anisotropic profile in platinum

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

2. Document ID: US 6323132 B1

L22: Entry 2 of 6 File: USPT Nov 27, 2001

US-PAT-NO: 6323132
DOCUMENT-IDENTIFIER: US 6323132 B1

TITLE: Etching methods for anisotropic platinum profile

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

3. Document ID: US 6277762 B1

L22: Entry 3 of 6 File: USPT Aug 21, 2001

US-PAT-NO: 6277762
DOCUMENT-IDENTIFIER: US 6277762 B1

TITLE: Method for removing redeposited veils from etched platinum

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

4. Document ID: US 6265318 B1

L22: Entry 4 of 6 File: USPT Jul 24, 2001

US-PAT-NO: 6265318
DOCUMENT-IDENTIFIER: US 6265318 B1

TITLE: Iridium etchant methods for anisotropic profile

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 5. Document ID: US 6087265 A

L22: Entry 5 of 6 File: USPT Jul 11, 2000

US-PAT-NO: 6087265
DOCUMENT-IDENTIFIER: US 6087265 A

TITLE: Method for removing redeposited veils from etched platinum

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 6. Document ID: US 6037264 A

L22: Entry 6 of 6 File: USPT Mar 14, 2000

US-PAT-NO: 6037264
DOCUMENT-IDENTIFIER: US 6037264 A

TITLE: Method for removing redeposited veils from etched platinum

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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Terms	Documents
L21 and stack	6

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